

TS-5600 User's Manual





Technologic Systems, Incorporated
16610 East Laser Drive, Suite 10
Fountain Hills, AZ 85268
480-837-5200
FAX 837-5300
info@embeddedx86.com
<http://www.embeddedx86.com/>

This revision of the manual is dated
March 2, 2004

All modifications from previous versions are listed in the appendix.

Copyright © 1998-2003 by Technologic Systems, Inc. All rights reserved.

Limited Warranty

Technologic Systems warrants this product to be free of defects in material and workmanship for a period of one year from date of purchase. During this warranty period Technologic Systems will repair or replace the defective unit in accordance with the following instructions:

- Contact Technologic Systems and obtain a Return Material Authorization (RMA) number and a copy of the RMA form.
- Fill out the RMA form completely and include it and dated proof of purchase with the defective unit being returned. Clearly print the RMA number on the outside of the package.

This limited warranty does not cover damages resulting from lightning or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Technologic Systems be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

Repairs made after the expiration of the warranty period are subject to a flat rate repair charge and the cost of return shipping. Please contact Technologic Systems to arrange for any repair service.

Table Of Contents

LIMITED WARRANTY.....	II
1 INTRODUCTION	5
2 PC COMPATIBILITY.....	5
2.1 Operating Systems	5
3 POWER.....	6
4 MEMORY.....	6
4.1 SDRAM.....	6
4.2 Flash.....	6
4.3 Compact Flash cards.....	6
4.4 Using the SanDisk USB Compact Flash Card Reader.....	7
4.5 Non-Volatile SRAM.....	7
5 SERIAL PORTS.....	8
5.1 Serial Port Configuration Registers	8
5.2 Serial Port Hardware.....	8
5.3 RS-485 Support.....	9
5.4 Automatic RS-485 TX Enable.....	9
5.5 Adding Serial Ports.....	10
6 DIGITAL I/O.....	11
6.1 DIO Header.....	11
6.2 Using LCD Port as Digital I/O.....	11
7 ANALOG INPUTS AND OUTPUTS	12
7.1 SPI Interface.....	12
7.2 A/D Converter Interface.....	13
7.3 DAC Converter Interface.....	14
8 LCD INTERFACE	15
9 MATRIX KEYPAD SUPPORT.....	16
10 THE 10/100 BASE-T ETHERNET PORT.....	17
10.1 LINUX TCP/IP configuration	17
10.2 DOS TCP/IP configuration – Packet Driver and WATTCP	18
10.3 WATTCP.CFG configuration file.....	18
10.4 DOS TCP/IP configuration – MS Client for DOS.....	18
11 PCMCIA BRIDGE	19
11.1 Hardware	19
11.2 Software (Linux support only)	19
11.3 Supported Devices	20
12 SPI BUS	21
12.1 Hardware	21
13 REAL TIME CLOCK.....	22
14 WATCHDOG TIMER	23
15 LED, JUMPERS AND EXTERNAL RESET	24
16 PC/104 BUS EXPANSION.....	25
17 LOADING OR TRANSFERRING FILES	26
17.1 Developing with the Technologic Systems TS-9500.....	26
17.2 Transferring files with Compact Flash.....	26
17.3 Zmodem Downloads.....	26
18 DEBUGGING.....	27
18.1 Integrated BIOS Debugger	27
18.2 Using other debuggers	27
19 VIDEO, KEYBOARD, AND CONSOLE REDIRECTION	28
20 SYSTEM BIOS SETUP SCREENS	29
20.1 Main CMOS Configuration Screen.....	29
20.2 Basic CMOS Configuration	30
20.3 Adding a TS-9400 or TS-9500 with Compact Flash	30
20.4 Custom CMOS Configuration	31

20.5 Shadow Configuration..... 32

21 FEEDBACK AND UPDATES TO THE MANUAL 32

APPENDIX A - BOARD DIAGRAM AND DIMENSIONS 33

APPENDIX B - OPERATING CONDITIONS 33

APPENDIX C - SYSTEM MEMORY MAP 34

APPENDIX D - SYSTEM I/O MAP 35

APPENDIX E - BIOS INTERRUPT FUNCTIONS 36

 Int 15h / Function B000h - Technologic Systems BIOS information 36

 Int 15h / Function B010h - LED Control 36

 Int 15h / Function B042h – Alphanumeric LCD Support 37

 Int 15h / Function B040h – Matrix Keypad Support..... 37

 Int 15h / Function A1h – Console I/O Redirection 37

 Int 15h / Function B050h – A/D Converter Control..... 38

 Int 15h / Function B020h - Jumper Pin Status 38

APPENDIX F - USING A HIGHER RATE (10X) BAUD CLOCK..... 39

APPENDIX G - FURTHER REFERENCES 40

APPENDIX H - MANUAL REVISIONS 40

1 Introduction

The model TS-5600 is a compact, full-featured PC compatible Single Board Computer based on the AMD Elan520 processor. At 133 MHz, it is approximately 10 times faster than our other 386EX based products for only a small additional cost. PC compatibility allows for rapid development since you can use standard PC development tools such as Turbo C or Power Basic or Linux based tools as well. If you have done work in the PC world in the past, you will find you can now build applications for a very small target that does not require a keyboard, video, floppy disks, or hard drives.

By adding the optional TS-9500 daughter board, you can compile and debug directly on the TS-5600 with standard VGA video and keyboard interfaces. Alternatively, you can typically write and debug code on a host PC using standard development tools for the PC platform, then simply copy it to and run it on the TS-5600 without modification. If additional peripherals are required, the PC/104 expansion bus allows for many standard functions available off-the-shelf. It is also very simple to create a custom PC/104 daughter board for those special features that differentiate your product. Technologic Systems can provide technical support as well as a free quotation for any custom hardware, software, or BIOS modifications you may require.

This manual is fairly short. This is because for the most part, the TS-5600 is a standard x86-based PC compatible computer, and there are hundreds of books about writing software for the PC platform. The primary purpose of this manual is documenting where the TS-5600 differs from a standard PC.

2 PC Compatibility

PC compatibility requires much more than just an x86 processor. It requires a PC compatible memory map and I/O map as well as a PC compatible BIOS. The General Software EMBEDDED BIOS offers a high degree of compatibility with past and present BIOS standards allowing it to run off-the shelf operating systems software and application software.

The EMBEDDED BIOS has been tested with all major versions of DOS, including MS-DOS, DR-DOS, and Embedded DOS 6-XL; all major versions of OS/2, including MS-OS/2 and IBM OS/2; MS-Windows 3.1, Windows-95, Windows NT, and NetWare 386.

2.1 Operating Systems

Technologic Systems Embedded PCs are compatible with a wide variety of x86-based operating systems. A partial list OSes currently used with our boards by customers includes:

- TNT Embedded Toolsuite, Phar Lap Software
- UCos II
- RTKernel, On Time Software
- RTEMS, On-Line Applications Research Corporation
- DOS with WATTCP, public domain TCP/IP source code for DOS
- Linux

The TS-5600 is shipped, free of charge, with Embedded DOS ROM by General Software.

The TS-5600 can be shipped upon request with Linux pre-installed for a nominal fee. The Linux file system and kernel is also freely available on the web should you wish to install it yourself. Typically, the Linux OS requires a 16MB or larger Compact Flash or an M-System's DiskOnChip.

3 Power

The TS-5600 requires **regulated** 5VDC at 800 mA (typical maximum). When running the Linux OS, it will drop to about 300 mA during low usage. A quick release [screw-down terminal block for the 5V power and power GND connections](#) is provided for easy connection to an external power supply.

When power is first supplied to the TS-5600, the board mounted LED is immediately turned on under hardware control. Once the processor begins execution, the LED is turned off. The LED then turns on then off to provide a characteristic blink during execution of POST. If the LED does not turn on at all, the most likely problem is the power supply. Check that the +5V and GND connections are not reversed. A diode protects the board against damage in such a situation, but it will not run.

Please note that supply voltages over 6 VDC may damage the TS-5600.

Be sure to use a **regulated** 5 VDC power supply, preferably with current limiting to 3 to 5 Amps. If using a PC power supply that may be capable of supplying 20 Amps or more, it is possible to do irreversible damage if the polarity on the power leads is reversed.

4 Memory

4.1 SDRAM

The TS-5600 has a total of 32 Megabytes (MB) of high-speed SDRAM providing 640 Kilobytes (KB) of base memory, 31 MB of extended memory, and 128 KB of shadow RAM for the BIOS. This is identical to a standard PC memory map. The TS-5600 can be ordered with 64MB of SDRAM, but it is not field upgradeable.

The TS-5600 SDRAM chips are soldered directly to the board. By not using a SIMM socket, the TS-5600 is much more reliable in high-vibration environments.

4.2 Flash

There is a total of 2 MB of Flash memory on the TS-5600 with 128 KB reserved for the BIOS. During POST, this 128 KB area is copied from Flash into SDRAM at addresses E0000h through FFFFFh for improved performance (a standard technique known as BIOS Shadowing). The remainder of the Flash memory (1920 KB) is configured as a solid-state disk (SSD) drive appearing as drive A. Drive A is fully supported by the BIOS as an INT 13h drive.

The physical Flash memory is accessed by the BIOS in protected mode at memory address 148M.

The ~~Flash~~ **LASH** memory is guaranteed capable of a minimum of 100,000 write/erase cycles. This means that if you [completely erase and rewrite](#) to the ~~SSD~~ **Flash** drive 10 times a day you have over 27 years before any problems would occur. [Reading the SSD produces no wear at all.](#)

Power failure during flash writes can cause corruption of flash drive FAT tables (A: or B:). Therefore applications writing frequently should use a Compact Flash card drive which is much more tolerant of power failures during write cycles.

Flash drive A is **read-only** when JP3 is not installed. Removing JP3 also makes the 128 kbyte BIOS area of the Flash write protected as well. Write protecting the A: drive can be useful if there are critical files in the final product that must be very secure.

4.3 Compact Flash cards

If 2MB of Flash is insufficient for your application, additional non-volatile storage can be added with a Compact Flash (CF) card. CF cards can supply additional storage that will behave much as a hard drive does in a typical PC with sizes ranging from 8MB to 512MB. These products are inherently more rugged than a hard drive since they are completely solid-state with no moving parts.

The Compact Flash card has the added advantage of being removable media. A SanDisk USB Compact Flash reader/writer (which is included in the TS-5600 Developer's Kit) is recommended for the host PC for file transfers. This results in the ability to quickly move files from a host PC to the TS-5600 using a Compact Flash card as the removable media. Since the Compact Flash card appears as a standard IDE drive on the TS-5600, it uses no additional RAM for drivers. While a USB Compact Flash reader allows for hot swapping of the Compact Flash card on the host PC, the Compact Flash interface on the TS-5600 is not hot swappable, the TS-5600 must be rebooted after removing or installing a Compact Flash card.

4.4 Using the SanDisk USB Compact Flash Card Reader

This device allows for a very fast and reliable method of moving files between the host PC and target SBC (TS-5600). The Compact Flash (CF) card can then be hot swapped (inserted or removed without rebooting the host PC). Sometimes it is necessary to unplug the USB cable and reinstall it after swapping CF cards (at least Windows ME seems to prefer this).

Note: The TS-5600 always needs to be powered off before swapping CF cards.

4.5 Non-Volatile SRAM

An optional 32 KB of non-volatile SRAM memory can be installed into the TS-5600. This behaves exactly like battery-backed SRAM. Non-volatile SRAM provides non-volatile memory with unlimited write cycles and no write time degradation, unlike Flash memory. The SRAM uses an additional 32 KB memory range of D0000h through D7FFFh. If the SRAM is installed, PC/104 daughter card that uses memory mapped I/O must not conflict with this address range.

5 Serial Ports

The two PC compatible asynchronous serial ports (COM1 and COM2) provide a means to communicate with external serial devices such as printers, modems, etc. Each is independently configured as a standard PC COM port that is compatible with the National Semiconductor NS16C450. Alternatively, these ports can be changed to the 16C550 mode with 16 byte FIFOs in both the receive and transmit UART channels. COM1 appears in the I/O space at 3F8h – 3FFh and uses IRQ4. COM2 is located at 2F8h – 2FFh and uses IRQ3.

By changing an internal configuration register in the Elan520, the serial clock to the COM ports can be switched to a 10 times rate (18.432 MHz). This feature allows baud rates higher than 115 Kbaud (such as 230K baud or 576K baud), as well as non-standard lower baud rates (such as 24 Kbaud). See Appendix G for further information.

The COM1 and COM2 ports may also be configured to use a DMA channel, which may be useful when very high baud rates are being used.

See the AMD Elan520 User's Manual for further details.

5.1 Serial Port Configuration Registers

Because both serial ports are 100% PC compatible, software written for the PC that accesses serial ports directly or through standard BIOS calls will work without modification on the TS-5600. The details of the COM port internal registers are available in most PC documentation books or the data sheet for the National Semiconductor NS16C550 may be consulted.

See the AMD Elan520 User's Manual for further details.

5.2 Serial Port Hardware

The COM2 RS-232 port has 7 signals supported: RXD, TXD, RTS, CTS, DTR, DSR, and DCD. This port can interface to almost any RS-232 device. The COM1 RS-232 serial port has 4 signals supported: RXD, TXD, RTS and CTS. This is quite sufficient to interface with the vast majority of serial devices. The TS-5600 COM ports are accessible on two 10-pin Headers labeled COM1 and COM2. Adaptor cables are available to convert these into standard 9-pin Sub-D male connectors.

	5V Power	10	5	GND	
	NC	9	4	DTR	[out]
[in]	CTS	8	3	TXD	[out]
[out]	RTS	7	2	RXD	[in]
[in]	DSR	6	1	DCD	[in]

Figure 1 – **COM2** Serial Port Header Pin-out

	5V Power		5	GND	
	Rx -	9	4	Rx +	
[in]	CTS	8	3	TX data	[out]
[out]	RTS	7	2	RX data	[in]
	Tx -	6	1	Tx +	

Figure 2 – **COM1** Serial Port Header Pin-out

PLEASE NOTE: The serial port headers use a non-standard numbering scheme. This was done so the header pins would have the same numbering as the corresponding DB-9 pin; i.e. pin 8 (CTS) on the header connects to pin 8 on the DB-9

PLEASE NOTE: COM1 has connections for the RS-232 port and the RS-485 port on the same 10-pin header, only one of the two functions will be used at a time.

The pin-outs for the COM1 and COM2 10-pin headers are listed above.

When using COM1 in the RS-232 mode, be sure that the jumper labeled “232” is installed.

5.3 RS-485 Support

An option is available to add support to COM1 for half duplex or full duplex RS-485. RS-485 drivers allow communications between multiple nodes up to 4000 feet (1200 meters) via twisted pair cable. Half-duplex RS-485 requires one twisted pair plus a Ground connection, while full duplex requires two twisted pair plus a Ground.

For half-duplex operation, a single twisted pair is used for transmitting and receiving. Bit 6 at I/O location 75h must be set to enable RTS mode or bit 7 can be set to enable Automatic mode. In RTS mode, the serial port RTS signal controls the RS-485 transmitter/receiver (See Automatic mode below). When RTS is asserted true, the RS-485 transmitter is enabled and the receiver disabled. When RTS is de-asserted the transmitter is tri-stated (disabled) and the receiver is enabled. Since the transmitter and receiver are never both enabled, the serial port UART does not receive the data transmitted.

For full-duplex operation, two twisted pairs are used and the transmitter can typically be left on all the time. Simply use RTS mode, and set RTS true.

See Figure 2 above for connector pin-outs.

Note: the correct jumper (FD or HD) must be installed. See the Table 2 for details.

Fail-safe bias resistors are used to bias the TX+, TX- and RX+, RX- lines to the correct state when these lines are not being actively driven. This is an important consideration, since in a typical RS-485 installation, the drivers are frequently tri-stated. If fail-safe bias resistors are not present, the 485 bus may be floating and very small amounts of noise can cause spurious characters at the receivers. 4.7KΩ resistors are used to pull the TX+ and RX+ signals to 5V and also to bias the TX- and RX- signals to ground. Termination resistors may be required for reliable operation when running long distances at high baud rates. Termination resistors should only be installed at each end of an RS-485 transmission line. In a multi-drop application where there are several drivers and/or receivers attached, only the devices at each end of the transmission line pair should have termination resistors.

A read at I/O location 75h bit 1 will return a "1" when the RS-485 option is installed.

5.4 Automatic RS-485 TX Enable

TS-5600 boards support fully automatic TX enable control. This simplifies the design of half-duplex systems since turning off the transmitter via the RTS signal is typically difficult to implement. The COM1 UART transmit holding register and the transmit shift register both must be polled until empty before deasserting RTS when using the RTS mode. The design gets more difficult when using the TX FIFO or when using a multi-tasking OS such as Linux.

In Automatic mode, Timer2 and a Xilinx PLD keep track of the bits shifting out the COM1 UART. This circuit automatically turns on/off the RS-485 transceiver at the correct times. This only requires the TIMER2 to be initialized once based on baud rate and data format, and bit 7 at I/O location 75 must be set. A utility called AUTO485.exe is included in the AUTOEXEC.bat that simplifies this task.

RS-485 Quick start procedure:

1. The RS-485 option must be installed
2. Install FD jumper for full-duplex or HD for half-duplex RS-485 operation
3. Attach the RS-485 cable to the 10-pin Header - Adaptor cables to Sub-DB9 connector are available from Technologic Systems
4. Set the COM1 UART serial parameters (baud rate, data, parity, and stop bits, interrupts, etc).
5. Run Auto485.exe utility (configures bits 6 and 7 at I/O 75h) (and initializes Timer2)
6. For Half-Duplex RTS mode:
To transmit data, assert RTS and write the data to the UART.
To receive data, deassert RTS and read the data from the UART
7. For Half-Duplex Automatic mode: just read or write data to the UART

Jumper	Receiver Source
FD	Full-Duplex RS-422
HD	Half-Duplex RS-485
232	RS-232

Table 1 – COM1 Receiver Source

5.5 Adding Serial Ports

If your project requires more than two serial ports, additional ports may be added via the PC/104 expansion bus. Technologic Systems offers three different daughter boards (TS-SER1, TS-SER2, and TS-SER4) that add 1,2,or 4 extra COM ports respectively. Typically these would be configured as COM3 or be assigned other higher COM I/O locations. Because DOS only directly supports four serial ports, any additional ports beyond four will require software drivers if using DOS.

The TS-5600 PC/104 bus has IRQ 5, 6, 7, 9, 12 or 15 available for additional serial ports.

Note: IRQ7 is used by many PCMCIA cards.

Typically each serial port has a dedicated interrupt, but the TS-SER4 allows all four extra serial ports to share a single interrupt. This is very helpful in systems with a large number of serial ports since there are a limited number of IRQ lines available.

6 Digital I/O

There are 23 Digital Input/Output (DIO) lines available on the TS-5600. These are available on two headers labeled DIO and LCD. In addition to the DIO signals, each header also has 5 Volt power and Ground available, while the DIO header has an external reset available on pin 12 and IRQ6 in available on pin 13. The header labeled LCD can be used as 11 DIO lines or as an alphanumeric LCD interface (See Section 7). Most of the DIO lines are arranged as byte-wide ports that can be programmed as either inputs or outputs in groups of 4-bits.

Four of the DIO lines are dedicated 0-5V swing outputs with high current drive capability. Two of these outputs can sink or source 25 mA, while the other two can sink or source 100 mA.

The 5V power output pins on these headers have a 750 mA Poly-Fuse to prevent excessive current.

6.1 DIO Header

The DIO port provides +5V, GND, and 12 digital I/O lines that may be used to interface the TS-5600 with a wide range of external devices. DIO lines DIO_0 thru DIO_7 are a byte-wide port accessed at I/O location Hex 7E, while the 4 other DIO lines DIO_8 thru DIO_11 are accessed in the lower 4 bits of I/O location Hex 7F. I/O location Hex 7D is a control port for DIO. The direction of DIO lines DIO_0 thru DIO_3 is controlled by bit 0 of I/O location Hex 7D, and the direction of DIO_4 thru DIO_7 is controlled by bit 1 of I/O location Hex 7D. The DIO_8 thru DIO_11 lines are always outputs. In all cases, when a control bit is a "1", it is setting the corresponding DIO lines to be Outputs, while a "0" sets them to be Inputs. All control bits at I/O location Hex 7D are initialized at reset to be "0".

5 V	16	15	DIO_7
IRQ6	14	13	DIO_6
Reset#	12	11	DIO_5
DIO_11	10	9	DIO_4
DIO_10	8	7	DIO_3
DIO_9	6	5	DIO_2
DIO_8	4	3	DIO_1
GND	2	1	DIO_0

Figure 2 – DIO Header Pinout

The DIO_0 thru DIO_7 digital outputs on this port can source 4 mA or sink 8 mA and have logic swings between 3.3V and ground. The digital inputs have standard TTL level thresholds and must not be driven below 0 Volts or above 5.0 Volts. DIO lines DIO_0 thru DIO_5 have 4.7K Ω pull-up resistors to 5V biasing these signals to a logic "1". DIO_6 and DIO_7 are not biased and may float to either state when configured as Inputs, if not being actively driven.

DIO_10 and DIO_11 outputs have very high current drivers and can source or sink 100 mA each. DIO_8 and DIO_9 outputs can source or sink 25 mA. DIO_8 thru DIO_11 all swing between 0 and 5V. Pin 14 on the DIO header is connected directly to IRQ6 (also available on the PC/104 bus).

Pin 12 is an active low reset signal. It has a 4.7K pull-up resistor to 5V. A logic low on this signal will cause a hard reset to the TS-5600 (same as a power cycle).

It is possible change the DIO_11 output so that it is driven by the Timer2 signal. The Timer2 signal has historically been used to drive the speaker in a PC. The DIO_11 output has 100 mA source and sink drive capability, so it could be used to directly drive a small 8 ohm speaker if a series capacitor is used to block the DC component and a series resistor is added to reduce the power out. A 47 μ F capacitor and a 27 ohm resistor is a good starting point (adjust the resistor for volume).

If bit 2 at I/O location Hex 79 is set, Timer2 will drive the DIO_11 output (instead of bit 3 at I/O location Hex 7F).

6.2 Using LCD Port as Digital I/O

The LCD Port can be used as 11 additional digital I/O lines or it can be used to interface to a standard alphanumeric LCD display. At system reset, the port defaults to DIO mode. If using an LCD display this port can be switched to LCD mode by writing a "1" into bit 4 at I/O location Hex 7D, or the BIOS call to enable the LCD also sets bit 4 at I/O location Hex 7D (See Section 8 for LCD mode).

When the LCD port is in DIO mode, pins LCD_RS and LCD_WR are digital inputs, LCD_EN is a digital output, and LCD_0 thru LCD_7 are programmable as either inputs or outputs.

LCD_6	14	13	LCD_7
LCD_4	12	11	LCD_5
LCD_2	10	9	LCD_3
LCD_0	8	7	LCD_1
LCD_WR	6	5	LCD_EN
Bias	4	3	LCD_RS
GND	2	1	5V

Figure 5 – Pinout for LCD header when used as DIO

LCD_RS and LCD_WR can be read at I/O location 73h bits 7 and 6, respectively. The state of LCD_EN is controlled by writing to I/O location 73h bit 0.

LCD_0 thru LCD_7 can be read or written at I/O location 72h. The direction of this byte-wide port (pins 7 – 14) is determined by bits 2 and 3 at I/O location 7Dh. If bit 2 is a zero, then the lower 4 bits (pins 7 – 10) are inputs. If bit 2 is logic 1, then pins 7 – 10 are outputs. Bit 3 at location 7Dh controls the upper 4 bits, pins 11 – 14 in a like manner.

All digital outputs on this port can source 4 mA or sink 8 mA and have logic swings between 3.3V and ground. The digital inputs have standard TTL level thresholds and must not be driven below 0 Volts or above 5.0 Volts.

The 5V power has a 750 mA Poly-Fuse to limit the current.

7 Analog Inputs and Outputs

The TS-5600 supports an optional 8-channel, 12-bit A/D converter (ADC) and an optional 2-channel 12-bit Digital-to-Analog converter (DAC).

The A/D converter has a conversion time of 8 microseconds. Six of these channels (1-6) are available on the Analog Header. Channel # 7 monitors the 5V power on the TS-5600 while channel # 8 is connected to ground. The ADC is based on an Analog Devices AD7888 chip and uses a Texas Instruments LT1009 for the precision 0.2% reference voltage. The AD7888 chip has eight analog inputs with a 0-2.5V range. Analog channels 4-6 on the TS-5600 have a 0-2.5V analog input range. Analog channels 1-3 use resistor dividers to obtain 0-10V analog input ranges. All of the analog channels have a 100 nF capacitor at each analog input of the AD7888 chip. This creates a low pass filter with a bandwidth of approximately 500 Hz.

Channel # 7 has 6.19K and 4.32K ohm resistors creating a voltage divider being driven by the on-board TS-5600 5V supply. This divider results in 41.1% of 5V supply voltage driving the AD7888 analog input. If the 5V supply were exactly 5.000 Volts, this would result in the ADC reporting 82.2% of a full-scale reading. Put another way, a full-scale reading on the ADC would indicate that the 5V supply is at 6.083 Volts.

Pin	Range	Description
1	0 – 10V	Analog Chan. 1
3	0 – 10V	Analog Chan. 2
5	0 – 10V	Analog Chan. 3
7	0 – 2.5V	Analog Chan. 4
9	0 – 2.5V	Analog Chan. 5
11	0 – 2.5V	Analog Chan. 6
13	0 – 5V	DAC Channel 1
15	0 – 5V	DAC Channel 2
Even		Analog GND

Table 7 Analog Header

2	4	6	8	10	12	14	16
1	3	5	7	9	11	13	15

Figure 3 - Analog Header Pinout

7.1 SPI Interface

The SPI bus is a three-wire interface that allows high-speed serial communications using low-pin count peripherals. The A/D converter and the DAC chip are both accessed using the SPI bus. The SPI bus is a byte-oriented bus, so 16-bit transfers (required by the A/D and DAC chips) need to use two back-to-back byte transfer cycles. The SPI bus details are presented in Section 12.

7.2 A/D Converter Interface

The AD7888 chip uses the SPI bus for all data transfers. Prior to accessing the AD7888, the SPI control register must be set to Hex 21. This sets the SPI bus for the following format:

- 2 MHz clock rate
- Clock idle state is high
- Non-inverted phase
- MSB shifted first

Then the Chip Select for the AD7888 chip must be asserted low. The Elan520 DIO pin PIO27 controls the chip select to the AD7888. PIO27 can be set to a low state by writing a Hex 0800 to memory location Hex DFC3A.

An acquisition is initiated by sending a 16-bit word to the AD7888. The exact format of this 16-bit word is described below. To start the acquisition, the 8-bits of the command byte must be loaded into the SPI TX register, then a Hex 03 written into the SPI Command register will cause the MS byte to be sent to the AD7888. The SPI Status register bit 1 must be polled until it is zero to indicate the MS byte transfer is complete (takes about 4 microseconds with the 2 MHz clock). The RX data (MS byte) should be read at this time and stored, and then a zero should be written into the TX register, and again a Hex 03 is written into the SPI Command register. The SPI Status register bit 1 must be polled until it is zero to indicate the LS byte transfer is complete. Then the RX data register can be read to get the LS byte returned from the AD7888. When all A/D acquisitions are completed, the Chip Select for the AD7888 must be deasserted by setting PIO27 to a logic high.

The 16-bits of RX data received is the A/D conversion result. The four MS bits are always zero and the lower 12-bits represents the analog value of the sampled channel. The total time for a single acquisition is approximately 8 microseconds.

The command byte that is sent to the AD7888 chip determines how the next acquisition is taken. The command byte is the first 8-bit quantity sent to the AD7888.

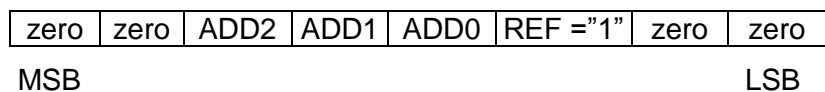


Figure 4 – A/D Command Byte Format

Bits 3-5 determine which of the 8-channels is sampled, and bit 2 determines whether the internal or external reference is used. Bit 2 should always be set to "1" to indicate an external reference is to be used.

Due to the design of the AD7888 chip, it is not possible to select the channel to convert and also convert the selected channel in a single 8 microsecond acquisition cycle. The AD7888 uses a pipelined architecture where the channel being converted is determined by the value of bits 3-5 for the previous cycle. This means that to sample a random analog channel, it will require two complete cycles, the first cycle to get the desired channel selected, and the second cycle to acquire the analog value. In most cases, this is not necessary, since you will always be sampling a known set of channels and can create an algorithm that pipelines the acquisitions.

A Linux driver has been written for the A/D converter, the Linux A/D driver with full "C" source code can be found on our website. Refer to the "Linux Developers Manual" on the Technologic Systems website: www.embeddedx86.com

7.3 DAC Converter Interface

The DAC uses a Texas Instruments TLV5618A chip with a 3 microsecond conversion time. It has two 12-bit DAC outputs that have an analog voltage range of 0-5V. The DAC also uses the same Texas Instruments LT1009 for the precision 0.2% reference voltage that is used for the A/D converter.

The TLV5618A chip uses the SPI bus for all data transfers. Prior to accessing the TLV5618A, the SPI control register must be set to Hex 03. This sets the SPI bus for the following format:

- 8 MHz clock rate
- Clock inverted (idle state = 0)
- Non-inverted phase (data latched on falling edges)
- MSB shifted first

Then the Chip Select for the TLV5618A chip must be asserted low. The Elan520 DIO pin PIO15 controls the chip select to the AD7888. PIO15 can be set to a low state by writing a Hex 8000 to memory location Hex ????.

Any write to the DAC register will in

Any write to the DAC register will initiate a DAC cycle with the lower 12-bits being the value written into one of the two DAC channels or into a buffer register. Bits 14,15 select the DAC channel (1-4) to be written into. Bit 13 allows the DAC value to be written into a Buffer register inside the TLV5617 chip. This buffer register acts as temporary holding register. This special cycle is implemented to allow

for a simultaneous update of two DAC channels. For example, if the Bit 13 is set and Bit 15 is clear, then the DAC cycle will update the buffer in the TLV5617, but will not change any analog output. Then when a DAC cycle is run writing to Channel 2, Channel 1 will be updated with the holding register value. Both Channel 1 and Channel 2 analog outputs will change at exactly the same time. Channels 3 and 4 can also implement this simultaneous update in the same manner except Bit 15 must be set for the buffer write cycle. If simultaneous updates are not required, always leave bit 13 clear and simply select one of the four channels with bits 14 and 15.

Bit 12 set selects a fast settling time of about 3 microseconds, while Bit 12 clear will select a slower 10 microseconds. Consult the TLV5618 data sheet for details. When using the slow settling mode, the analog output has a slighter greater current sink and source capability. So this may be more desirable than the faster settling time.

A Linux driver has been written for the DAC, the Linux DAC driver with full "C" source code can be found on our website. Refer to the "Linux Developers Manual" on the Technologic Systems website:

www.embeddedx86.com

Bits	Notes
Bits 0-11	Value to DAC
Bit 12	R0 (Select Register)
Bit 13	PWR (zero = Power On)
Bit 14	SPD (zero = Slow mode)
Bits 15	R1 (Select Register)

Bits	Notes
Bits 15, 12	R1, R0
0,0	Write to DAC B and Buffer
0,1	Write to Buffer only
1,0	Write to DAC A and Update DAC B with Buffer content
1,1	Reserved

8 LCD Interface

A 14-pin LCD connector is provided on the TS-5600 for interfacing with standard alphanumeric LCD displays. These displays use a common controller, the Hitachi HD44780 or equivalent. While software written for the HD44780 will work with all displays using the controller, the cable needed is dependent on the display used. For most displays, a straight-through type ribbon cable can be used. The connector on the LCD display is typically mounted on the backside of the display.

Warning – using an incorrect cable or mounting the LCD connector on the front-side can result in a reverse power polarity and can damage the LCD display. Please refer to your LCD data sheets for in-depth information.

Pin	Function	Comments
1	LCD 5V	
2	LCD GND	
3	LCD_RS	Register Select (Buffered A0)
4	Bias	680 Ohm to GND
5	LCD_EN	Active high Enable
6	LCD_WR#	Active low Write
7	LCD_D1	
8	LCD_D0	
9	LCD_D3	
10	LCD_D2	D0 – D7: Buffered bi-directional data bus
11	LCD_D5	
12	LCD_D4	
13	LCD_D7	
14	LCD_D6	

Table 3 - LCD Header Signals

The TS-5600 BIOS incorporates a fairly complete set of INT10h video routines that work with the LCD. Once the LCD has been enabled (**INT15h/Func B042h** – see Appendix E poniżej)

2	4	6	8	10	12	14
1	3	5	7	9	11	13

Figure 6 - LCD Header Pinout

The LCD can be written to as the standard I/O device. This means that software can be developed and debugged using standard I/O calls, and the executable will work with LCD, VGA video, or redirected COM port. See the section 16 for more information.

I/O addresses **72h** and **73h** are used to access the LCD. Figure 6 shows the header pin-out, while Table 3 lists the LCD signals. The section below will briefly describe the LCD interface signals. The LCD can be controlled directly by software at these addresses.

The register select signal is simply the buffered A0 address line. Thus, reads and writes to **72h** cause register select to be low, and those to **73h** cause it to be high. Generally the LCD uses this line to separate data bytes from command bytes. See your LCD data sheet for details.

The LCD Write# signal is an active low write enable line.

LCD Enable is an active high signal, raised whenever the LCD addresses are being read or written.

D0 – D7 are bi-directional, buffered copies of the data bus and carry all data and commands to the LCD.

Table 3 is not the standard pin-outs given for LCD displays. But this pin-out allows a standard ribbon cable to be used when the ribbon cable is attached to the **backside** of the LCD.

Example LCD code is available at: <http://www.embeddedx86.com/downloads/util.zip>

9 Matrix Keypad Support

The DIO2 port, signals DIO_0 through DIO_7, may be configured to support a 4 x 4 matrix keypad. When enabled, BIOS firmware performs all the work, making the matrix keypad appear as a simple 16-key keyboard to software. This allows the use of standard keyboard access routines. The default set of keys translated by the BIOS consists of 0 – 9, A – D, *, and #. The # key is returned as an ASCII Carriage Return character (Hex 0D). Because the user is writing the software, this set of keys is usually sufficient. However, a custom translation table can be loaded, allowing the use of function keys, arrow keys, or any other key on the keyboard.

Matrix keypad support is enabled or disabled using **INT15h, Function B040h** (see Appendix F). Once enabled, standard keyboard BIOS functions are enabled. Note that console redirection and the matrix keypad support are mutually exclusive – console redirection must be disabled to use the keypad.

A matrix keypad can be used with console redirection only if the keypad is not used as stdin, but read from as a hardware device. This is useful if one wishes to use console redirection or to use a keyboard as stdin. See section 16 for an explanation of console I/O and redirection. See the Technologic Systems download page for example code.

<http://www.embeddedx86.com/downloads/keypad.zip>

When using a matrix keypad, the DIO signals DIO_0 through DIO_7 are not available as general I/O.

A Linux driver has been written for the Matrix Keypad, the Linux driver with full “C” source code can be found on our website. Refer to the “Linux Developers Manual” on the Technologic Systems website: www.embeddedx86.com

10 The 10/100 Base-T Ethernet Port

The TS-5600 has a full-function IEEE 802.3 (10/100 Mbit/sec) Ethernet port provided by Davicom DM9102A Ethernet controllers. The DM9102A is a single-chip, 32-bit PCI Ethernet controller that includes such features as full-duplex operation, power saving shutdown modes, LED indicators for link status/activity (Green) and auto-sense network speed detection (Amber). The physical interface is 10/100Base-T (RJ45 connector).

The TS-5600 has both a LINK/ACTIVITY LED and a 10/100 speed LED built into each RJ-45 connector that indicates the current Ethernet status. The LINK LED (left side of connector, green) is active when a valid Ethernet link is detected. This LED should be ON whenever the TS-5600 is powered on and properly connected to a 10/100BaseT Ethernet network. The LINK/ACTIVITY LED will blink to indicate network activity either inbound or outbound. The SPEED LED (right side of connector, amber) will be on when a 100 Mbit network is detected and off for a 10 Mbit network. Both of these LEDs are controlled by the DM9102A and do not require initialization by the processor.

10.1 LINUX TCP/IP configuration

When using the TS-5600 with TS-Linux, the DM9102A driver can be included in the kernel or loaded as a kernel module. If the Technologic Systems kernel is used, the DM9102A driver is built into the kernel. The settings stored in EEPROM on the TS-5600 are used to configure the DM9102A.

The TCP/IP settings for the TS-Linux are configured in the file '/etc/sysconfig/ifcfg-eth0', here is a listing:

```
DEVICE=eth0           # Name of Ethernet interface
IPADDR=192.168.0.50   # IP address of this Ethernet interface.
NETMASK=255.255.255.0 # Used with NETWORK to determine local IP's.
NETWORK=192.168.0.0   # Used with NETMASK to determine local IP's.
BROADCAST=192.168.0.255 # Broadcast IP for system wide messages.
ENABLE=yes            # Initialize on startup
```

The TCP/IP network settings are configured in the file '/etc/sysconfig/network_cfg', here is a listing:

```
### Technologic Systems
### General Network Configuration File
###
NETWORKING=yes
GATEWAY=192.168.0.1   # Gateway for internet access
GW_DEV=eth0           # Gateway device to use
Hostname="miniepc.embeddedx86.com" # Host name for this computer
BOOTPROTO=no
DEFRAG_IPV4=no
FORWARD_IPV4=no
```

The TCP/IP name resolution server is configured in the file '/etc/resolv.conf', here is a listing:

```
Nameserver 192.168.0.1 # Name server for domain name lookups.
```

To access the web server, open a web browser and enter "192.168.0.50" as the address. This should display the sample web page which demonstrates some of the functionality of Apache with PHP. Use the "ifconfig" command at the bash prompt to display the status of the Ethernet ports. See the Technologic Systems Linux support page:

<http://www.embeddedx86.com/support/linuxhelp.php>

10.2 DOS TCP/IP configuration – Packet Driver and WATTCP

A standard packet driver for DOS is installed on the board as shipped, along with sample network applications written with the public domain Waterloo TCP/IP software (WATTCP). WATTCP is a freely available package (including source code) that provides TCP/IP connectivity for programs written for the DOS environment. See the Technologic Systems download page

<http://www.embeddedx86.com/downloads/wat2001t.zip>

In addition, we have written a simple DOS HTTP web server using WATTCP that is included on the TS-5600 utility disk. The simple web server uses CGI calls to control a DIO pin from a web browser. Full source code is included, and you are free to modify and extend the code for your own use on Technologic Systems Single Board Computers.

The DOS packet driver (DM9PCIPD.COM) is loaded by `AUTOEXEC.BAT` once DOS starts. Hardware settings are read from the EEPROM chips and used by the packet driver to initialize each DM9102A. Below is an example of the DOS command line to load a packet driver for the Ethernet interface:

```
DM9PCIPD 0X60
```

The TCP/IP settings for the WATTCP code are stored in the `WATTCP.CFG` configuration file in the `A:\ETHERNET` directory, this file must be modified for the network environment where the TS-5600 will be installed.

10.3 WATTCP.CFG configuration file

```
my_ip=192.168.0.20           // IP address of this Ethernet interface.
hostname="epc.embeddedx86.com" // Host name of this computer.
netmask=255.255.255.0       // Used to determine which IP's are local.
gateway=192.168.0.1         // Gateway for internet access.
nameserver=192.168.0.1      // Name server for domain name lookups.
```

With the `WATTCP.CFG` file properly setup and the 10/100 base-T cable connected, you should be able to ping other nodes on the network, i.e. `'ping www.embeddedx86.com'`

Other WATTCP examples include: serial to telnet redirector, http file download, telnet server, and finger, web server with I/O control . Many more can be downloaded from the internet as freeware.

10.4 DOS TCP/IP configuration – MS Client for DOS

The Davicom Ethernet adapter has the MS Client for DOS driver available. This has been tested and found to work on Windows workgroups as well as Samba workgroups. Check the Technologic Systems web page for driver downloads (www.embeddedx86.com).

Email support@embeddedx86.com with questions.

11 PCMCIA Bridge

11.1 Hardware

The TS-5600 uses a Texas Instruments PCI1510 single-slot CardBus controller designed to meet the PCI Interface Specification for PCI to CardBus Bridges. The PCI-to-CardBus controller supports a single PC card socket compliant with the PC Card Standard (rev. 7.2). The PC Card Standard retains the 16-bit PC Card specification defined in the PCI Local Bus Specification and defines the 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The TS-5600 supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

The PCI1510 is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during CardBus PC Card bridging transactions.

All card signals are internally buffered to allow hot insertion and removal. The PCI1510 is register-compatible with the Intel 82365SL-DF and 82365SL ExCA controllers. The PCI1510 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance.

The PCMCIA Bridge uses IRQ10 to monitor card plug events and IRQ7 is used for the PC Card interrupt.

11.2 Software (*Linux support only*)

Card Services for Linux is a complete PCMCIA support package. It includes a set of loadable kernel modules that implement a version of the PCMCIA 2.1 Card Services applications program interface, a set of client drivers for specific cards, and a card manager daemon that can respond to card insertion and removal events, loading and unloading drivers on demand. It supports "hot swapping" of PCMCIA cards, so cards can be inserted and ejected at any time.

The current package supports many ethernet cards, modems and serial cards, several SCSI adapters, most ATA/IDE devices, and some SRAM and FLASH memory cards. All the common PCMCIA controllers are supported, so it should run just about all Linux-capable devices.

The PCMCIA CS drivers are a standard install with the following changes to `/etc/pcmcia/config.opts`

REMOVED:

```
include port 0x0100-0x04ff, port 0x800-0x8ff
exclude irq7
```

ADDED:

```
exclude irq3
exclude irq4
exclude irq5
```

These changes will avoid trying to allocate the x100-x4ff region, which is unavailable to PCI devices in the TS-5600. And will force the use of IRQ7 for the PCMCIA device, which the PCMCIA Bridge chip has been programmed for in the BIOS during power up.

See `/etc/pcmcia` directory and the documentation on the sourceforge project page. (link below)

The home page for PCMCIA Card Services for Linux can be found @ <http://pcmcia-cs.sourceforge.net/>

11.3 Supported Devices

There is a very large list of devices supported by the Linux Card Services package available on the sourceforge page. Here is a list of devices tested at Technologic Systems and known to work with the TS-5600:

802.11b Wireless Ethernet adapters

- Belkin F5D6020 (16-bit version not CardBus version)
- Netgear MA401
- Orinoco Gold PC24E-H-FC
- Phoebe WLC010(INT)

Cellular Modem

- Novatel Merlin C201 Sprint PCS Connection Card

Hard Drives

- Toshiba MK5002MPL 5GB Hard Disk Drive
- Sandisk Compact Flash w/PCMCIA to Compact Flash Adapter

Modem

- Actiontec DataLink Fax/Modem

Ethernet adapters

- SoHoware ND5120-E 16-bit 10 Mbps adapter
- Netgear FA511 32-bit CardBus 10/100 adapter
- Hawking Technology 32-bit CardBus 10/100 adapter

12 SPI Bus

12.1 Hardware

The SPI bus is a three-wire interface that allows high-speed serial communications using low-pin count peripherals. The A/D converter, the DAC chip, and the EEPROM (holds BIOS configuration data) are all accessed using the SPI bus. The SPI bus is a byte-oriented bus, so 16-bit transfers (required by the A/D and DAC chips) need to use two back-to-back byte transfer cycles.

The SPI bus is available on a 10-pin header. Table 7 and Figure 5 document the Header pin-outs. Additional off-board chips may be added to the SPI bus.

Warning: The TS-5600 has several chips using the SPI bus. Some of these chips are running at 3.3V and are not 5V tolerant. This means that any devices that are added to the SPI bus must not drive the SPI data input (pin 5) any higher than 3.3V. Alternatively, a 5V device can be added if a series resistor (470 ohm) is added to the SPI Data input line to limit the current.

Pin	Description
1	SPI Data (out)
2	5V Power
2	SPI CLK (out)
4	GND
5	SPI Data (in)
6	GND
7	PIO4 (Chip Select)
8	PIO5 (Chip Select)
9	PIO6 (Chip Select)
10	PIO7 (Chip Select)

Table 7 SPI Bus Header

There are 5 registers that control the Elan520 SPI bus:

Control Register	Address = DFCD0h
TX data Register	Address = DFCD1h
RX data Register	Address = DFCD4h
Command Register	Address = DFCD2h
Status Register	Address = DFCD3h

2	4	6	8	10
1	3	5	7	9

Figure 5 – SPI Bus Header Pinout

Sample drivers are available for the A/D converter and the DAC. These can be quite useful to help create drivers for other devices.

13 Real Time Clock

The TS-5600 has a standard PC compatible real-time clock (RTC) that is built into the Elan520 CPU. This clock has no battery-backup, which means it is volatile, and must be initialized after power is applied. If a non-volatile battery-backed RTC is required, the TS-5620 daughter board can be added to provide this capability. The TS-5620 is a very low-cost option that is only 1.1 x 3.5 inches (2.8 x 9.0 cm) and uses an ST Micro M48T86PC1 module for the real-time clock function. This module contains the lithium battery, 32.768 kHz crystal, and a RTC chip with 114 bytes of battery-backed CMOS RAM. It is guaranteed to maintain clock operation for a minimum of 10 years in the absence of power.

Both the internal RTC and the TS-5620 RTC are totally compatible with the Motorola 146818 chip used in the original PC. It is located at the standard PC I/O addresses of Hex 070 and 071. The top 48 bytes (index 50h through 7Fh) are not used by the BIOS and are available for user applications. However, since the TS-5600 uses an EEPROM to make this data non-volatile, a special method must be used to make any user data non-volatile. If you wish to use this area for non-volatile storage, contact Technologic Systems for details.

The CMOS RAM that is located inside the RTC chip is used to hold all of the BIOS set-up parameters. This RAM is always non-volatile even when using the internal RTC. All of the set-up parameters are stored in a non-volatile EEPROM chip. The data stored in the EEPROM is copied into the CMOS RAM during every boot cycle. This is all totally transparent and appears to operate as a standard CMOS set-up RAM.

The schematic for the TS-5620 is posted on our website. The TS-5620 design only uses two chips. This circuitry can be freely used on any customer daughter board design if the battery-backed RTC feature is necessary.

The TS-5600 internal RTC is capable of generating a square wave output function with a period of 500 mSec to 122 uSec. The TS-5620 RTC does not have access to IRQ8 and can not implement this function. The internal RTC square wave output pin is connected to IRQ8 on the processor, and can be used to generate periodic interrupts. The keypad example code uses this function to generate interrupts at a 256 Hz rate.

<http://www.embeddedx86.com/downloads/keypad.zip>

14 Watchdog Timer

Bits 0-7	Timeout Value
01h	0.5 milliseconds
02h	0.5 seconds
04h	1 second
08h	2 seconds
10h	4 seconds
20h	8 seconds
40h	16 seconds
80h	32 seconds

Table 4 Watchdog Timer Timeout Values

Bit Position	Function
Bit 15	1 = Enable WDT
Bit 14	1 = Generate Reset at Timeout 0 = Generate Interrupt at Timeout
Bit 13	Must always be 0
Bit 12	1 = WDT Interrupt has occurred (Interrupt routine must clear this bit)
Bits 8-11	Must always be 0
Bits 0-7	Timeout Value (See Table 4)

Table 5 – WDTMRCTL Register

Register	Memory Address
WatchDog Control (WDTMRCTL)	DFCB0h
WDT Counter Bits 0-15 (Read only)	DFCB2h
WDT Counter Bits 16-31 (Read only)	DFCB4h
WDT Interrupt Mapping	DFD42h

Table 6 - WatchDog Timer Memory Map

The AMD Elan520 contains a 32-bit watchdog timer (WDT) unit that can be used to prevent a system “hanging” due to a software failure. The WDT can be programmed to cause an interrupt or a full system reset when the WDT times out allowing a guaranteed recovery time from a software error. To prevent a WDT timeout, the application must periodically “feed” the WDT by writing a “clear-count key sequence” to the Watchdog Timer Control (WDTMRCTL) register.

The WDT must be initialized with the timeout period desired. This may be as short as 0.5 mS or may be as high as 32 seconds. After the WDT has been enabled, the 32-bit watchdog counter starts counting from zero. The application software can reset this counter at any time by writing a “clear-count key sequence” to the WDTMRCTL. If this counter reaches the timeout period, then an interrupt is generated, or a system reset occurs.

If programmed to cause an interrupt, the WDT must be fed within the next timeout period or else a system reset occurs as an additional failsafe feature.

In order to load the WDTMRCTL register, a specific sequence of three word writes is required. A 3333h, followed by CCCCh, followed by the value to be loaded into the WDTMRCTL register must be written to the WDTMRCTL register.

In order to clear the WDT counter (feeding the watchdog), a “clear-count key sequence” must be written to the WDTMRCTL register. This is a specific two word write sequence with a write of AAAAh, followed by a write of 5555h. (Writing this “clear-count key sequence” has no effect on the contents of the WDTMRCTL register)

Typically a system reset at timeout is the preferred method for using the WDT, if you wish to have an interrupt occur before the system reset occurs (bit 14 = 0 in the WDTMRCTL Register), additional programming is required to “attach” a specific IRQ to the WDT. An interrupt service routine must also be written to handle this IRQ. Please see the AMD Elan520 User's Manual or contact Technologic Systems.

When using the Linux OS, we provide a driver to initialize and “feed” the WDT. We also provide a Linux sample application program with full source.

If using DOS, the following sample of Turbo C code (real-mode DOS) will enable the WDT with a 4 second timeout period :

```
int main() {
    unsigned int far *wdtctrl ;
    wdtctrl = (unsigned int far *) MK_FP (0XDF00, 0X0CB0);
    *wdtctrl = 0x3333;
    *wdtctrl = 0xCCCC;
    *wdtctrl = 0xD010 ;      /* 0xD0 = Enable WDT to Reset Mode, 0x10 = 4 second timeout */
    printf (“System will reset in 4 seconds”);
    return 0;
}
```

15 LED, Jumpers and External Reset

Jumper	Function
JP1	Automatic CMOS - CMOS memory is reset every time the system boots, IDE0 and IDE2 Compact Flash are automatically detected and configured in the BIOS Configuration menu.
JP2	Enable Serial Console - Default to COM2. (unless JP6 installed)
JP3	Write Enable Drive A – Remove this jumper to write protect Flash drive A:
JP4	Fast Console - Console is set to 115K baud. (defaults to 9600 baud)
JP5	User Jumper - Read using BIOS call or directly in I/O space. (See appendix D & E)
JP6	Console on COM1 (requires JP2 installed to enable console)

Table 7 - Jumper Listing

The TS-5600 has an LED available for user software. The user LED may be used for diagnostics, status messages, and simple output. When power is first supplied to the TS-5600, the user LED is immediately turned on under hardware control. Once the processor begins execution, the LED is turned off, then flashed on and off again briefly. After boot, this LED can be used for user applications. The state of the LED is complemented by any activity to the Compact Flash card. (accesses to the CF causes the LED to flicker)

The status of all jumpers except JP3, can be read at I/O location 77 (See Table 12).

BIOS interrupt functions can be used to interface software with the user LED and option jumpers. Please see Appendix F for further details and the utility disk for example code.

The LED can be also accessed at I/O location 77h bit 0. A Logic “1” is LED on condition.

The CF activity signal is exclusive ORed with the control bit at I/O location 77h. This causes the LED to always flicker when there is access to the CF card.

The DIO pin 12 is connected in parallel with the on-board power reset chip. See the DIO section for details. Pulling DIO pin 12 low will perform a ‘cold’ boot.

16 PC/104 Bus Expansion

The PC/104 is a compact implementation of the PC/AT ISA bus ideal for embedded applications. Designers benefit from using an already-developed standard, rather than creating their own. Further, the presence of a compact form-factor PC compatible standard has encouraged the development of a broad array of off-the-shelf products, allowing a very quick time to market for new products.

Pin #	Signal Name
A1	IRQ1†
A2 - A9	D7 through D0
A10	IOCHRDY
A11	AEN
A12 - A31	A19 through A0
A32	GND
B1	GND
B2	RESETDRV
B3	+5V
B4	IRQ9
B11	SMEMW#
B12	SMEMR#
B13	IOW#
B14	IOR#
B15	Reserved †
B16	Reserved †
B17	DACK1#
B18	DRQ1
B19	User Chip Select# †
B20	SYSCLK (8.25 MHz)
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	NC
B25	NC
B27	TC
B28	BALE
B29	+5V
B30	OSC (14.3 MHz)
B31	GND
B32	GND

Table 8 - **Supported** PC/104 Signals on the 8-bit Bus

† these signals have a non-standard usage.

The electrical specification for the PC/104 expansion bus is identical to the PC ISA bus. The mechanical specification allows for the very compact implementation of the ISA bus tailor made for embedded systems. The full PC/104 specification is available from the IEEE Standards Office under # IEEE P996.1 (see Appendix E for further information). Basically, this bus allows multiple daughter boards in a 3.6 inch by 3.8 inch form factor to be added in a self-stacking bus. Since the electrical specs are identical (except for drive levels) to a standard PC ISA bus, standard peripherals such as COM ports, Ethernet, video, LCD drivers, and Flash drives may be easily added using standard drivers.

The TS-5600 implements a sub-set of the 8-bit or optionally the 16-bit version of the PC/104 bus. We have found this allows the support of the vast majority of PC/104 boards including all of the above mentioned examples.

IRQ3 and IRQ4 are typically used by COM2 and COM1 and are not available on the PC/104 bus. If a daughter board must use either IRQ3 or IRQ4, it is possible to reconfigure the Elan520 registers and reassign IRQ lines. Contact us for details.

Pin B19 (normally not used) has been reassigned to be a User Chip Select. This active low signal decodes the I/O address range 140h through 15Fh, to allow for simple low-cost daughter board designs.

All Technologic Systems 3000 and 5000 series products will support the User Chip Select feature.

Memory range C8000-CFFFF is available for custom daughter boards to map into the memory space on the PC/104 bus. See section 17.4 on configuring the Custom CMOS settings.

Pin #	Signal Name
B5	-5V
B6	DRQ2
B7	-12V
B8	ENDXFR#
B9	+12V
B26	DACK2#

Table 9 - **Unsupported** PC/104 Signals

Pin #	Signal Name
C0	GND
C1	SBHE#
C2 - C8	LA23 - LA17
C9	MEMR#
C10	MEMW#
C11-18	D8 - D15
D0	GND
D1	MEM16#
D2	IO16#
D5	IRQ12
D6	IRQ15
	IRQ14
D7	(shared with CF)
D8	DACK0#
D9	DRQ0
D16	+5V
D18, D19	GND

Table 10 - Supported signals on the optional 16-bit PC/104

17 Loading or Transferring Files

Two methods are available for transferring files between a desktop PC and your TS-5600: Compact Flash and Zmodem downloads. Full descriptions of each are detailed below. Other programs that use serial ports to transfer should work as well (for example, FastLynx).

17.1 Developing with the Technologic Systems TS-9500

The TS-9500 daughter board provides full VGA video, keyboard, and mouse interfaces necessary to work within most environments. It also has a Compact Flash card that can be used even if the TS-5600 is using a Compact Flash card as well. You can transfer your development tools (e.g. Turbo C) onto the TS-9500 Compact Flash card. Now you can compile, debug, and execute right on the TS-5600 target.

17.2 Transferring files with Compact Flash

The TS-5600 removable Compact Flash card can be used to easily move files from a host system. We suggest using a low-cost SanDisk™ USB compact flash card interface for your host system. This is included in the TS-5600 Developer's Kit.

For best results, we have noticed that it is best to boot the host PC with a Compact Flash card installed in the SanDisk USB Reader. The Compact Flash card can then be hot swapped (inserted or removed without rebooting the host PC).

There are two other options for connecting a Compact Flash to your host computer. A Compact Flash to PCMCIA adapter, which can map a Compact Flash as a hard drive on your laptop host computer. Or, a Compact Flash to IDE adapter, which connects to the 40 pin IDE interface on your host computer. The IDE adapter will allow you can boot to CF, run fdisk, format, etc.

17.3 Zmodem Downloads

Using the Zmodem protocol to send files to and from the TS-5600 is simple and straightforward. The only requirement is a terminal emulation program that supports Zmodem, and virtually all do. If you are using Windows 95 or later for your development work, the HyperTerminal accessory works well.

To download a file to the TS-5600 from your host PC, execute `DL.BAT` at the DOS command line on the TS-5600 (while using console-redirectation from within your terminal emulator) and begin the transfer with your terminal emulator. In HyperTerminal, this is 'Send File...' from the 'Transfer' menu.

To upload a file from the TS-5600 to your host PC, execute `UL.BAT <FILENAME>` at the DOS command line on the TS-5600 and start the transfer in your terminal emulator. Many emulators, HyperTerminal among them, will automatically begin the transfer themselves.

Occasionally there may be errors in transmission due to background solid-state disk operations. This is not a problem -- Zmodem uses very accurate CRC checks to detect errors and simply resends bad data. Once the file transfer is complete the file is completely error free.

For best results when using HyperTerminal, the hardware handshaking must be enabled in HyperTerminal. To increase the download speed you could also use a ram disk on the TS-5600 to receive the download file, and then copy to the flash drive.

To declare a ram disk insert this line into the config.sys file: `device=\dos\vdisk.sys /kbtouse=1024`

Please note that the utility used to perform Zmodem file transfers on the TS-5600 side is called DSZ, produced by Omen Technologies. **DSZ is shareware -- it is not free.** If you decide to use it, you are legally obligated to pay Omen Technologies. Currently the cost is \$20. Further info is available in the DSZ zip file located on the utility disk, and contact info for Omen Technologies is in Appendix G.

18 Debugging

There are two main methods for debugging on the TS-5600: using the integrated BIOS debugger (INT3) and/or using your development tool's debugger (this usually requires the TS-9500 video and keyboard).

18.1 Integrated BIOS Debugger

To provide simple, direct access to the TS-5600 hardware, the system BIOS has an integrated debugger that can perform standard low-level debugger functions. The debugger allows you to perform operations such as disassemble code, display and alter the contents of memory, write to and read from I/O ports, and single-step through or breakpoint code. The debugger is not intended for use as the only debugging tool for applications, but it can be a real lifesaver when you need interactive, direct access to hardware.

The BIOS debugger can be entered by any of several methods:

- The debugger hooks the CPU exception vectors in case a divide by zero occurs, an invalid opcode is executed, or an INT 3 instruction is executed, for example. By placing an INT 3 instruction in your application code the debugger will automatically be invoked. To resume, type the 'G' command to "GO", or continue on with the rest of initialization.
- From DOS-ROM by typing 'INT3' at the command prompt. If the full command.com interpreter is running, this is an internal command. If only mini-command.com is running, this will execute a small utility that simply contains an 'INT 3' instruction.
- From the BIOS Setup main menu (started by typing 'ctrl-C' during the BIOS POST), the **ENTER SYSTEM BIOS DEBUGGER** selection will enter the debugger. After use, typing the 'G' (go) command will return to the SETUP screens.
- As a boot action, as a last-ditch effort if the operating system cannot be booted from the appropriate drives or out of ROM.

A complete discussion of debugger commands is available in the *Integrated BIOS Debugger Reference Manual*, included on the TS-5600 Utility Disk and also available from the Technologic Systems web site. Entering '?' will list all available commands, and a 'g' (go) will return execution to the point where the debugger was called.

18.2 Using other debuggers

For example, the Turbo C debugger can be used on the target board using the TS-9500 video and keyboard interfaces. Any other standard PC software debugger of your choice should work just as well.

19 Video, Keyboard, and Console Redirection

The TS-5600 has no video controller or keyboard interface. This was done to keep the board size small and the cost low. For applications that require it, a PC/104 video board can be added to the system easily. Technologic Systems recommends the TS-9500, a PC/104 daughter board with video, keyboard, mouse, and compact flash. This is extremely useful in speeding up the development phase and shortening the time to market. With the TS-9500 installed, developers can develop right on the target board with any compiler or debugger of their choice (such as the Turbo C compiler or debugger).

Without a video board in the system, the TS-5600 can redirect all console activity to the COM2 serial port. Simply connect an ANSI terminal (or emulator) to COM2 with a null modem cable, using serial parameters of 9600 baud, 8 data bits, no parity, 1 stop bit, and make sure jumper **JP2** is installed. (JP4 will change the console to 115.2K Baud) All text information that would normally be displayed on a video screen is now displayed in your terminal window, and any serial data sent to the TS-5600 is seen as standard keyboard input by programs.

Please note that the console redirection support is limited by the fact that there is no actual video or keyboard hardware on the TS-5600. Programs must use the standard BIOS routines for display and keyboard input, which are rerouted to the serial port. Any program that accesses the video or keyboard hardware directly will not work. Keyboard redirection is limited simply because most of the extended keys on the keyboard (function keys and Alt key in particular) are not sent by the terminal emulator. For these reasons, the console redirection feature is meant more for system development, testing, and field repair, rather than as the primary user interface for a finished product.

If your application uses COM2, removing the jumper **JP2** easily disables console redirection.

If you wish to use a different serial port and / or baud rate for the console, the `CONSOLE.EXE` utility allows these modifications to be made. Please see the appropriate application notes for further details, available on the utility disk or from the Technologic Systems web site.

<http://www.embeddedx86.com/downloads/AP-100.pdf>

If a video board is installed on the PC/104 bus, the video BIOS on the graphics card will automatically replace the standard video routines (INT10h), disabling both the LCD display and the console redirection to COM2, regardless of the state of jumper **JP2**. If a video board is present, all console input is disabled and the TS-5600 will only accept input from a standard PC keyboard.

If LCD and/or Matrix keypad is enabled, the console must be directed to standard I/O. If a TS-9500 is present, with video/keyboard enabled the standard output will be directed to video, even if the LCD is enabled, if the Matrix keypad is enabled the PC keyboard and the Matrix keypad will work at the same time.

20.2 Basic CMOS Configuration

The "Basic CMOS Configuration" screen allows setup of the Compact Flash or IDE drives, Drive Assignment mapping and Boot Order, as well as Time, Date and misc. keyboard and memory test settings. The default settings for the TS-5600 are show below.

```

+-----+
|                                     |
|               System Bios Setup - Basic CMOS Configuration               |
|               (C) 2000 General Software, Inc. All rights reserved         |
+-----+-----+-----+-----+
| DRIVE ASSIGNMENT ORDER: | Date:>Dec 14, 2001 | Typematic Delay   : 250 ms |
| Drive A: 5300 Flash A:  | Time: 09 : 56 : 21 | Typematic Rate    : 30 cps |
| Drive B: 5300 Flash B:  | NumLock: Disabled | Seek at Boot      : None   |
| Drive C: Ide 0/Pri Master | Show "Hit Del"    : Enabled |
| Drive D: (None)         | BOOT ORDER:       | Config Box        : Enabled |
| Drive E: (None)         | Boot 1st: Drive C: | F1 Error Wait     : Enabled |
| Drive F: (None)         | Boot 2nd: Drive A: | Parity Checking   : (Unused) |
| Drive G: (None)         | Boot 3rd: DOS-ROM  | Memory Test Tick  : Enabled |
| Drive H: (None)         | Boot 4th: (None)   | Test Above 1 MB  : Enabled |
| Drive I: (None)         | Boot 5th: (None)   | Debug Breakpoints: Enabled |
| Drive J: (None)         | Boot 6th: (None)   | Splash Screen     : (Unused) |
| Drive K: (None)         |
+-----+-----+-----+-----+
| Boot Method: Boot Sector | IDE DRIVE GEOMETRY: Sect Hds Cyls | Memory |
+-----+-----+-----+-----+
| FLOPPY DRIVE TYPES:     | Ide 0: 2 = AUTOCONFIG, PHYSICAL    | Base:   |
| Floppy 0: Not installed  | Ide 1: Not installed                | 640KB  |
| Floppy 1: Not installed  | Ide 2: Not installed                | Ext:   |
|                           | Ide 3: Not installed                | 31MB   |
+-----+-----+-----+-----+
|                                     |
|                                     | ^E/^X/<Tab> to select or +/- to modify |
|                                     | <Esc> to return to main menu          |
|                                     |

```

The factory defaults shown will first attempt to boot from Compact Flash as Drive C:. If no CF is installed the BIOS will then boot from Drive A:. If a CF is installed, but it is not desired to boot from this drive, change the "Boot 1st" setting to "Drive A:".

In order for the Compact Flash to function properly as an IDE hard drive, the IDE DRIVE GEOMETRY must be set to "AUTOCONFIG, PHYSICAL" and the DRIVE ASSIGNMENT ORDER must be set to "Ide 0/Pri Master" or "Ide 2/Sec Master".

In this example the Compact Flash socket on the TS-5600 (Ide 0) is set as "AUTOCONFIG, PHYSICAL" and mapped so that drive C: is assigned to "Ide 0/Pri Master". This drive is also set as the 1st boot device.

20.3 Adding a TS-9400 or TS-9500 with Compact Flash

A TS-9500 may be added to the system, this board has its own Compact Flash socket which may be set to Primary Master or Secondary Master using the DIP switches. If the TS-9500 CF is set to Primary Master (DIP switch 5 on), then no CF card may be installed in the TS-5600 CF socket and the CMOS settings should be exactly as shown above. The TS-9500 CF card will be mapped as Drive C: and will be the boot drive. If the TS-9500 CF card is set to Secondary Master (Ide 2), then the TS-5600 CF socket may have a CF installed as Primary Master (Ide 0). To configure the TS-9500 as Secondary Master (DIP switch 5 off), change the IDE DRIVE GEOMETRY for "Ide 2" to "AUTOCONFIG, PHYSICAL" and change the DRIVE ASSIGNMENT for Drive D: to "Ide 2, Sec Master".

20.4 Custom CMOS Configuration

```

+-----+
|                                     |
|               System BIOS Setup - Custom Configuration               |
|      (C) 2000 General Software, Inc. All rights reserved              |
+-----+-----+
|                                     |
| Write Buffer           :>Disabled   | Cache Mode             : Write-Through |
| CPU speed             : 133 MHz    | C8000-CFFFF maps to  : PC/104 Bus  |
| GP Bus Timings       : Normal      | PNP IO Port 0A79h    : PCI Bus    |
|                                     |
|                                     |
+-----+-----+
|                                     |
|               ^E/^X/<Tab> to select or +/- to modify                 |
|               <Esc> to return to main menu                          |
|                                     |
+-----+
    
```

Write Buffer When write buffering is 'Enabled' the internal 16K byte L1 cache is used to allow zero wait state writes to SDRAM . This setting defaults to Disabled and may be 'Enabled' by the user to optimize performance.

Refer to the AMD Elan SC520 users manual section 11 for more information on write buffering.

Cache Mode When set to Write-Through all writes to SDRAM will be updated in the internal cache as well as the SDRAM. When set to Write-Back only the internal cache is updated, the cache controller will determine when to flush cache to SDRAM. This setting defaults to 'Write-Through' and may be set to 'Write-Back' by the user to optimize performance.

Refer to the AMD Elan SC520 users manual section 8.4.2.2 for more information on cache mode.

CPU Speed This will set the clock speed for the CPU core. This can be set to '100 MHz' or '133 Mhz'. The default speed for commercial temperature products is 133 MHz, the default for industrial temperature products is 100 MHz. Changing this setting will not affect industrial temperature products because they are specified by AMD with a maximum clock speed of 100 MHz.

C8000-CFFFF maps to This setting allows a block of memory space to be mapped to either the PC/104 bus or the onboard SDRAM. This setting defaults to PC/104 bus.

GP Bus Timings This setting allows the PC/104 bus timing to be stretched to allow slower devices to operate. If Plug-N-Play boards are installed, or in the case of older PC/104 daughter cards setting this entry to 'Slow' may be desired. This setting defaults to 'Normal' which has been tested and found to work with the vast majority of boards.

PNP IO Port 0xA79 This setting allows the Plug-N-Play configuration address to be mapped to the PC/104 bus. The I/O space above 0x400 is mapped to the PCI bus by default. If a Plug-N-Play device is connected to the PC/104 bus change this setting to 'GP Bus'.

AMD Elan SC520 Users Manual may be found at:
http://www.embeddedx86.com/downloads/520_user.pdf

20.5 Shadow Configuration

```

+-----+
|                                     |
|               System BIOS Setup - Shadow/Cache Configuration           |
|               (C) 2000 General Software, Inc. All rights reserved       |
+-----+
| Shadowing           :>Chipset           | Shadow 16KB ROM at C000 : Enabled |
| Shadow 16KB ROM at C400 : Enabled       | Shadow 16KB ROM at C800 : Disabled|
| Shadow 16KB ROM at CC00 : Disabled      | Shadow 16KB ROM at D000 : Disabled|
| Shadow 16KB ROM at D400 : Disabled      | Shadow 16KB ROM at D800 : Disabled|
| Shadow 16KB ROM at DC00 : Disabled      | Shadow 16KB ROM at E000 : Enabled |
| Shadow 16KB ROM at E400 : Enabled       | Shadow 16KB ROM at E800 : Enabled |
| Shadow 16KB ROM at EC00 : Enabled       | Shadow 64KB ROM at F000 : Enabled |
|                                     |
|                                     |
|                                     |
|                                     |
+-----+
|                                     |
|               ^E/^X/<Tab> to select or +/- to modify                 |
|               <Esc> to return to main menu                           |
|                                     |
+-----+
    
```

The Shadow Configuration menu allows BIOS extension ROMs to be copied to SDRAM in upper memory regions to reduce access times. Execution directly from ROM is significantly slower than executing from SDRAM. The region from C000-C7FF is usually reserved for the video BIOS extension in a PC compatible system, shadowing is enabled to optimize the video BIOS functions. The region from E000-FFFF contains the embedded BIOS code in the TS-5600. This region is shadowed to optimize BIOS code execution and to allow reprogramming of the BIOS while the BIOS is executing out of SDRAM. Other regions can be shadowed as required by specific applications.

21 Feedback and Updates to the Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Technologic Systems web site (www.embeddedx86.com). These include manuals, application notes, programming examples, and updated software and firmware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers (and prospective customers) is the number one influence. If you have questions, comments, or concerns about your TS-5600 Embedded PC, *please let us know*. Details for contacting us are listed in the front of this manual.

Appendix C - System Memory Map

Resource	Starting Address		Size
	hex	decimal	
Linear Flash Chip	940000h	148M	2M
Unused			
Extended Memory (RAM)	100000h	1M	15M or 31M or 63M
BIOS (Shadow RAM)	E0000h	896k	128k
Elan520 Configuration Registers	DF000h	892k	4k
PC/104 Bus	D8000h	864k	28k
NV SRAM	D0000h	832k	32k
PC/104 Bus or SDRAM (user configurable in CMOS setup, see sec. 17.4)	C8000h	800k	32k
PC/104 (typically video BIOS)	C0000h	768k	32k
PC/104 (typically video memory)	A0000h	640k	128k
Lower Memory (RAM)	00000h	00000	640k

Figure 4 – TS-5600 Memory Map

Appendix D - System I/O Map

The following table lists the I/O addresses used by the system. This is all a very standard PC compatible I/O map. All other I/O locations from 100h through 3FFh are available on the PC/104 expansion bus.

Hex Address	Resource
400h - FFFFh	PC/104 Bus (Not recommended for use)
3F8h – 3FFh	COM1
3F6h – 3F7h	Primary IDE (Compact Flash)
3E8h – 3EFh	Reserved for COM3
3B4h – 3DFh	Video (TS-9500)
376h – 377h	Secondary IDE (TS-9500)
2F8h – 2FFh	COM2
2E8h – 2EFh	Reserved for COM4
278h – 27Ah	Reserved for LPT1
1F0h – 1F7h	Primary IDE (Compact Flash)
198h – 19Fh	Registers on TS-9500
195h – 197h	Reserved for A/D Converter
170h – 177h	Secondary IDE (TS-9500)
140h – 15Fh	User Chip Select (PC/104 Bus)
080h – 0FFh	Internal Elan520 peripherals
074h – 07Fh	DIO and Control registers
072h – 073h	LCD port
070h – 071h	RTC and CMOS memory
060h – 064h	Keyboard Controller (TS-9500)
000h – 05Fh	Internal Elan520 peripherals

Table 11 – TS-5600 I/O Map

The I/O ranges of 100h – 13Fh and 200h – 26Fh are excellent choices for PC/104 daughter board I/O usage. When designing a custom PC/104 daughter board, a User Chip Select is available on PC/104 Bus pin B19 that decodes the I/O range 140h – 15Fh. This can make for a simpler and more cost-effective design.

I/O Address	R / W	Resource
74h	Read	Product Code 20h = Product Code for TS-5600
75h	Read	Bit 0 = Always set
	Read	Bit 1 = RS-485 Option
	Read	Bit 2 = Always zero
	R/W	Bit 6 = Enable RTS for RS-485
	R/W	Bit 7 = Enable Automatic RS-485
76h	Read	Bit 0 = External Reset Option (always)
	Read	Bit 1 = Industrial Temp. Range Option
77h	R/W	Bit 0 = LED (1 = ON)
	Read	Bit 1 = JP1
	Read	Bit 2 = JP2
		Bit 3 = Reserved
	Read	Bit 4 = JP4
	Read	Bit 5 = JP5
	Read	Bit 6 = JP6
78h		Reserved
79h	R/W	Bit 2 set = Timer2 drives DIO_11
7Ah		Reserved
7Bh		Reserved
7Ch		Reserved
7Dh	R/W	Control Register for DIO and LCD Bit 0 = Direction of DIO_0 – DIO_3 Bit 1 = Direction of DIO_4 – DIO_7 Bit 2 = Direction of LCD_0 – LCD_3 Bit 3 = Direction of LCD_4 – LCD_7 Bit 4 = Enable LCD Mode Bit 5 = Always Logic "1" Bit 6 = Always Logic "0" Bit 7 = Always Logic "1"
7Eh	R/W	DIO_0 thru DIO_7 (Bits 0-7)
7Fh	R/W	DIO_8 thru DIO_11 (Bits 0-3)

Table 12 – TS-5600 DIO and Control Registers

Appendix E - BIOS Interrupt Functions

We have extended the standard BIOS interrupts with several functions that simplify interfacing with the TS-5600 hardware.

Many books are available with detailed information on using interrupts with just about any language. Example code is also available on the utility disk.

You can download the complete "User's Manual with BIOS Interrupt Reference" from the Technologic Systems website: <http://www.embeddedx86.com/downloads/EBIOS-UM.PDF>

Int 15h / Function B000h - Technologic Systems BIOS information

This function is mostly for our own internal use, but may be useful for user programs as well. For example, your program could have debugging code that executes on your desktop machine, but does not when the program is executing on the TS-5600.

ENTRY:

AX = B000h

EXIT:

CY = 0 (carry flag)

AH = 0

AL = SP_VERSION

For standard versions of the BIOS, this is 0. An 'SP number' is assigned when custom modifications are made to the BIOS for a client, and it is returned in this register. Contact us for further information. (00h for standard products)

BH = BIOS Version, Major Number.

E.g. If the current BIOS version is 2.40, the register will contain 02h.

BL = BIOS Version, Minor Number.

E.g. If the current BIOS version is 2.40, the register will contain 28h (28h = 40 decimal).

CH = Base Flash Memory Size / 512kB

The TS-5600 is available with 1024kB of base Flash memory standard, but this can be increased to 2048 KB for custom orders. These would be returned as 02h or 04h, respectively.

CL = 50h

This is the hardware model number (50h = 80 decimal).

DX = Always returns: 'TS' (5453h)

Int 15h / Function B010h - LED Control

This function is used to turn the board LED on and off. You can also invert the LED, i.e. if the LED is off, it will be turned on, and if it is on it will be turned off.

ENTRY:

AX = B010h

BH = 00 - LED off.

01 - LED on.

81 - LED invert.

EXIT:

CY = 0 (carry flag)

AH = 00

Int 15h / Function B042h – Alphanumeric LCD Support

This routine enables and disables the console on the LCD interface. It supports all LCD displays sized 2 x 40 or smaller using a Hitachi HD44780 controller.

ENTRY:

AX = B042h
 BH = 00 - Disable LCD
 01 - Enable LCD
 02 - Return current LCD status

EXIT:

CY = Set if error, else clear if success (carry flag)
 AH = 00 - No Error / LCD initialized OK
 BH = 00 - LCD currently disabled / Not present
 01 - LCD currently enabled and running.

Int 15h / Function B040h – Matrix Keypad Support

This function is used to enable and disable support for the matrix keypad. When enabled, the RTC periodic interrupt (IRQ8 / INT70h) is enabled at 256 Hz and hooked to the keypad scanning routine. Disabling the keypad reverses this process – IRQ8 is turned off, and INT70h is returned to the original standard BIOS function. The default translation table consists of the following: 0 - 9, A - D, *, and # (# returns the scan-code for Carriage Return). A custom translation table is 16 words long, where each word is a scan code / ASCII pair for a key. Information on scan codes can be found in books on IBM PC hardware. Example programs are included on the utility disk. See Section 9 for further details.

ENTRY:

AX = B040h
 BH = 00 - Disable matrix keypad
 - Enable matrix keypad
 - Enable matrix keypad with a custom translation table
 CX = Translation table segment (if BH = 11)
 DX = Translation table offset (if BH = 11)

EXIT:

CY = 0 (carry flag)
 AH = 00

Int 15h / Function A1h – Console I/O Redirection

This function specifies the device that will be used by the BIOS to direct console input (INT 16h) and console output (INT 10h). If the LCD or Matrix keypad is to be used as the console, you must also call the LCD and/or Matrix keypad BIOS function to enable them.

ENTRY:

AX = A1h
 BH = 00 - Console is directed to Standard I/O. (VGA/keyboard or LCD/Matrix)
 01 - Console is redirected to COM1
 02 - Console is redirected to COM2
 03 - Console is redirected to COM3¹
 04 - Console is redirected to COM4

EXIT:

CY = 0 if success, set if failure (carry flag)

AH = 00 if no error, 86h if no supported by BIOS

Int 15h / Function B050h – A/D Converter Control

Function B050h provides a simple interface for performing a single A/D conversion. In case of hardware failure (or the ADC option is not present), a time-out returns an error code within approximately 50 μS.

ENTRY:

AX = B050h
 BL = Value to write into A/D Control register (See Table 6)

EXIT:

CY = 0 (no error)
 AH = 00 - No Error
 01 - bad subfunction
 02 - bad input registers (i.e. if BL bit 5 set)
 03 - ADC option not present (I/O 7Dh bit 0 = 0)
 04 - Hardware error (A/D timeout)
 BX = A/D Conversion value
 The ADC automatically sign-extends the result to the full 16 bits in bipolar mode, and masks the upper 4 bits in unipolar mode.

Int 15h / Function B020h - Jumper Pin Status

This function returns the status of the option jumpers in register BX according to the list below.

ENTRY:

AX = B020h

EXIT:

CY = 0 (carry flag)
 AX = 0
 BX = Jumper Pin Status. If Bit X = 1, the jumper is installed.

BX Bit	Jumper	Description
0	JP1	Auto CMOS configuration
1	JP2	Console Redirected to COM port
2	JP3	Write enable Flash A:
3	JP4	Console set to 115K baud
4	JP5	User definable
5	JP6	Console to COM1

Table 13 - Int15h/Function B020h register BX return values

Appendix F - Using a Higher Rate (10x) Baud Clock

The COM1 and COM2 serial port baud rate generator clock can be independently switched between either the standard 1.8432 MHz clock or a ten times rate of 18.432 MHz clock.

Changing to the 10x rate allows baud rates higher than 115.2 kbaud (such as 230.4 kbaud or 1152 kbaud), as well as, non-standard lower baud rates (such as 24 kbaud).

The baud rate clock for each COM port is controlled by bit 2 in the UART Control Register (UART1CTL and UART2CTL):

```
UART1CTL @ DFCC0h
UART2CTL @ DFCC4h
```

Clearing bit 2 to a "0" will change the clock to the 10X rate.

NOTE: You **must not** modify the other bits of this register. You **must** use a read-modify-write procedure to change these bits.

The following code written in Turbo C provides an example for changing COM1 to run at a 10X Baud rate:

```
int main () {
    unsigned char far *comreg;
    unsigned char comvalue;
    comreg=(unsigned char far *) MK_FP (0xDF00, 0xCC0);

    comvalue = *comreg;          /* Load Register */
    comvalue = comvalue & 0xFB /*Modify it*/
    *comreg = comvalue;         /*Write it out*/

    return 0;
}
```


Appendix G - Further References

Technologic Systems Web Site

<http://www.embeddedx86.com/>

Crystal CS8900A Ethernet Controller Overview

<http://www.cirrus.com/products/overviews/cs8900a.html>

Dallas Semiconductor DS12887 Data Sheet

<http://www.embeddedx86.com/downloads/12887.pdf>

Intel 386EX User's Guide

<http://developer.intel.com/design/intarch/manuals/272485.htm>

Maxim Integrated Products

<http://www.maxim-ic.com/>

National Semiconductor NS16C450 Data Sheet

Omen Technologies

<http://www.omen.com/>

PC/104 Consortium Web Site

<http://www.pc104.org/>

Waterloo TCP/IP Software (WATTCP)

<http://www.wattcp.com/>

Appendix H - Manual Revisions

01-10-03	Initial release
03-02-04	Fixed typo in section 6